CLOCK GATING FLIP-FLOP USING EMBEDDED XOR CIRCUITRY

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ABSTRACT

Flip flops/Pulsed latches are one of the main contributors of dynamic power consumption. In this paper, a novel flip-flop (FF) using clock gating circuitry with embedded XOR, GEMFF, is proposed. Using post layout simulation with 45nm technology, GEMFF outperforms prior state-of-the-art flip-flop by 25.1% at 10% data switching activity in terms of power consumption.

KEYWORDS

Dynamic power, low supply voltage, flip-flop.

1. INTRODUCTION

While the human brain consumes a little energy but can work with remarkable speed and response at real time, processors in data centers and personal computers would consume considerable energy. The System on Chip design integrates billions of transistors on one chip. However, current cooling equipment has a limited capability for removing the excess heat. Hence, one of the major challenges for digital systems is to minimize power consumption.

The clocking system consisting of clock distribution network and flip-flops (FFs) [1-7] consumes a large portion of dynamic power. In server processors, flip-flops take up to 20% of the total dynamic power of the processors. Hence FFs have become one of the dominant contributors to dynamic power [1].

In FFs, the dynamic power consumption is highly related clocking power consumption. There are different low power flip flops in the literature, for example, Transmission Gate FF (TGFF) [2], Topologically Compressed FF (TCFF) [3], Change Sensing FF(CSFF) [4], Static Contention Free FF (SC^2FF) [8]. TGFF uses two phase clocks and consumes clocking power even when data does not change. TCFF cannot work at low voltage due to reduced voltage swing at internal nodes. SC^2FF has a dynamic node which consumes power. CSFF reduces clocking power consumption by sensing whether input changes or not. When input does not change, there will be no redundant transition in CSFF. However, CSFF uses many stages which causes large DQ delay and there is still room to further reduce clocking power.

To further reduce power consumption, a change detect FF is proposed in this paper.

This paper describes the proposed fine-grained clock-gate FF in section II. Section III presents simulation results and an overall conclusion is presented in section IV.

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2. PROPOSED CLOCK GATING FLIP-FLOP

We propose a fine-grain clock-gate flip-flop using embedded XOR circuitry, GEMFF, as shown in Figure 1.

Clock gating control of GEMFF is built by employing a 'compare' block, consisting of NMOS N5, N6, N7, and N8, implementing a logic XOR function D⊕Q in terms of transistor ON/OFF operation, embedded in the pull down clock network.

When D does not change, Q remains the same as D, the 'compare' block turns off and stops clock propagation, the output will keep its value.

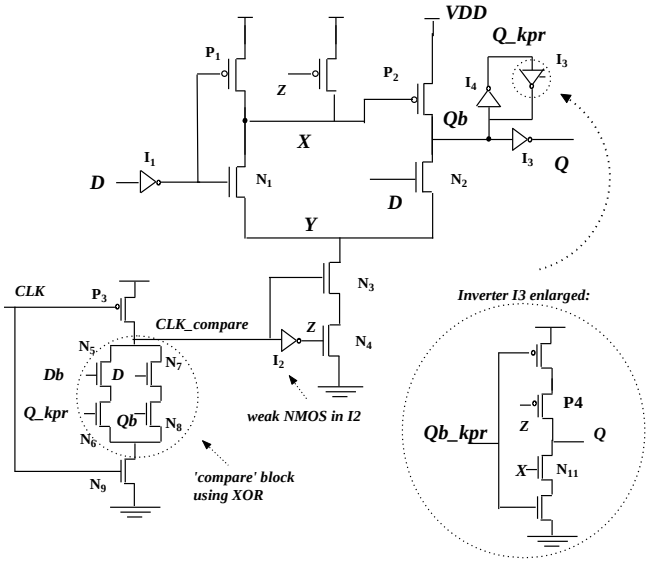

Figure 1. Proposed flip-flop using clock gating circuitry with embedded XOR, GEMFF

When D changes, XOR block turns ON, so 'CLK_compr' discharges to '0' by the XOR network and sets Z to be '1' and turns N4 ON.

Following that when CLK falling edge comes, 'CLK_compr' rises to '1' and turns N3 ON while N4 will stay ON for a short time until Z falls to '0', hence both N3, N4 will be ON for a short time which produces the pulse during which D is sampled.

The pulse width is determined by the delay of inverter, I2. A weak NMOS transistor is used in I2 to produce longer delay in order to have a wide pulse width. A larger gate length(multi times of 50nm) is used in that NMOS in I2. When that NMOS is weak, it will turn the transistor N4 off slowly. GEMFF is a negative clock edge triggered flip-flop.

3. SIMULATION RESULTS

The simulation results have been obtained from post-layout simulation in 45nm CMOS technology at room temperature using Hspice. The parasitic capacitances were extracted from the layouts. VDD is 1.0 V, and the clock frequency is 500 MHz. The setup used in our simulations is as follows. In order to obtain accurate results, we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the

output is required to drive an output of 4 standard sized inverters. Standard values are used for the sizes of PMOS and NMOS transistors, respectively.

The total power consumption includes the power consumption of flip–flop as well as the power consumption of the clock driver and the data driver.

Table 1 shows comparison of the flip-flop characteristics in terms of the number of total transistors, number of clock related transistors, number of clocked transistors switching during data idle time in a flip-flop, low voltage operation, redundant- transition-free, the transistor width, CQ delay, setup time, hold time and power consumption under switching activity of 5%, 10% and 20%, respectively.

Table 1. Comparing the FFs in Terms of the Number of Transistors, CQ Delay, and POWER

	Transistor count	**Total transistor width (um)**	**CQ (ps)**	**Set-up (ps)**	**Hold Time (ps)**	**Power (µw) 5% activity rate**	**Power (µw) 10% activity rate**	**Power (µw) 15% activity rate**
CSFF	24	5.16	46.3	92.2	-25.1	2.63	3.74	4.55
GEMFF	24	4.68	58.2	66.8	51.4	2.06	2.80	3.94

Figure 2 shows the power consumption comparison under different switching activities. The lower the switching activity, the more the power saving of GEMFF over CSFF. GEMFF consumes less power than CSFF by 21.8% and 25.1% at switching activities of 5% and 10%, respectively. Its power improvement over CSFF reduces to 13.5% at the switching activity of 15%.

Figure 3 shows the power consumption at different supply voltages from 0.4V to 1.0V. GEMFF has less power consumption over CSFF in all of the above voltages.

In terms of data-to-clock (DQ) delay, GEMFF's delay, 125.0 ps, is about 10% less than CSFF's delay, 138.5 ps.

In terms of PDP, CSFF's PDP is 5.11 fJ while GEMFF's PDP is 3.51 fJ at 10% switching activity. Hence, GEMFF has energy improvement over CSFF by about 30%.

Though power consumption has been improved in GEMFF, the hold time time is increased in GEMFF comparing with CSFF.

The above results demonstrate that GEMFF has lower power consumption than CSFF. Notice that GEMFF has larger hold time than CSFF, since GEMFF is a pulse triggered FF. This is a limitation of GEMFF.

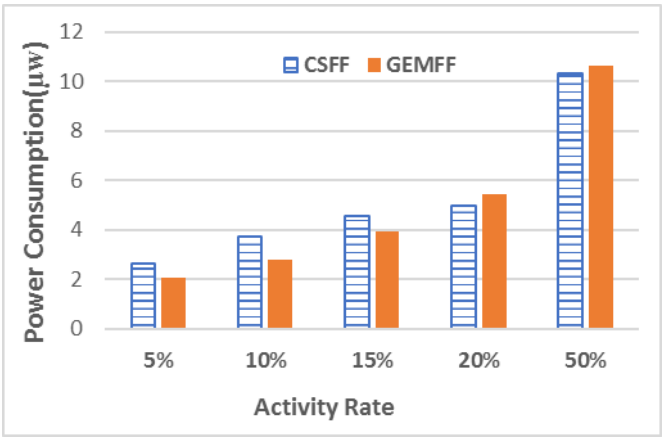

Figure 2. Power consumption under different switching activities: 5%- 50% @1.0V, 500 MHz

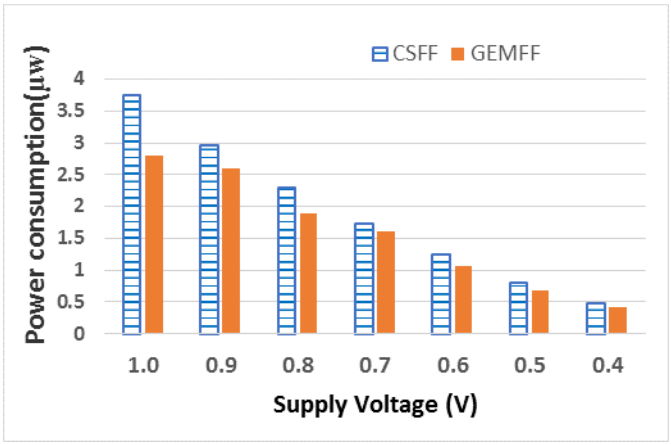

Figure 3. Power chart of different voltages 0.4V-1.0V at 10% switching activity, 500 MHz

4. CONCLUSIONS

In this paper, a novel flip-flop using clock gating circuitry with embedded XOR, GEMFF, is proposed. The new flip-flop uses clock gating to reduce redundant clock switching power. In view of power consumption, GEMFF outperforms CSFF by 25.1% at switching activity of 10%. Furthermore, at switching activities of 5% and 15%, GEMFF achieves less power consumption than CSFF as well. Hence GEMFF is applicable to achieve low power consumption.

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